Docket No. 303.632US1
WD #439121

Micron Ref. No. 99-0472

CLEAN VERSION OF PENDING CLAIMS

ELECTROSTATIC DISCHARGE PROTECTION DEVICE
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Serial No.: 09/648,919

Claims 1-7, 13, 17-29 and 33-35, as of June 26, 2002 (Date of Response to First Office Action).

1. (Amended) An electrostatic discharge (ESD) protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

2. The ESD protection device of claim 1, wherein the substrate comprises a first conductivity type and the first and second doped regions comprise a second conductivity type.

3. The ESD protection device of claim 1, wherein the substrate comprises a p-type conductivity material and the first and second doped regions comprise an n-type conductivity material.

4. The ESD protection device of claim 1, wherein first and second doped regions comprise a higher doping concentration than a doping concentration of the substrate.

5. The ESD protection device of claim 1 further comprising a first isolation structure placed on an opposing side of the first doped region from a region separating the first and the second doped regions, and a second isolation structure placed on an opposing side of the second doped region from a region separating the first and the second doped regions.

6. (Amended) An electrostatic discharge (ESD) protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein an amount current flowing between the first and second doped regions is not controlled by a voltage potential of a gate above the first and second doped regions.

7. (Amended) A gateless electrostatic discharge (ESD) protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region.

13. (Amended) An electrostatic discharge (ESD) protection device comprising:

a substrate; and

an implant within the substrate, the implant including two implant regions spaced apart by only the substrate region, wherein the substrate comprises a first conductivity type and the two implant regions comprise a second conductivity type, wherein conductivity between the two implant regions is not controlled by voltage potential of a gate above the two implant regions.

17. (Amended) An integrated circuit comprising:

a voltage source;

an external bonding pad; and

an electrostatic discharge (ESD) protection device connected between the bonding pad and the voltage source, the

ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

18. The ESD protection device of claim 17, wherein the substrate comprises a first conductivity type and the first and second doped regions comprise a second conductivity type.

19. The ESD protection device of claim 17, wherein the substrate comprises a p-type conductivity material and the first and second doped regions comprise an n-type conductivity material.

20. The ESD protection device of claim 17, wherein first and second doped regions comprise a higher doping concentration than a doping concentration of the substrate.

21. The integrated circuit of claim 17, wherein the voltage source is connected to ground.

22. The integrated circuit of claim 17, wherein the voltage source is connected to a voltage supply.

23. (Amended) An integrated circuit comprising:

a first voltage source;

a second voltage source;

an external bonding pad;

a first electrostatic discharge (ESD) protection device connected between the first voltage

source and the external bonding pad; and

a second ESD protection device connected between the second voltage source and the external bonding pad, wherein the second ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

24. The integrated circuit of claim 23, wherein the first voltage source is substantially smaller than the second voltage source.

25. The integrated circuit of claim 23, wherein the first voltage source is connected to ground.

26. The integrated circuit of claim 23, wherein the second voltage source is connected to a voltage supply.

27. (Amended) An integrated circuit comprising:

a voltage source;

an external bonding pad;

an internal circuit connected to the external bonding pad at a node; and

an electrostatic discharge (ESD) protection device connected between the node and the voltage source, the ESD protection device comprising:

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a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

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28. (Amended) An integrated circuit comprising:

a first voltage source;

a second voltage source;

an external bonding pad;

an internal circuit connected to the external bonding pad at a node;

a first electrostatic discharge (ESD) protection device connected between the first voltage source and the node;

and

a second ESD protection device connected between the second voltage source and the node, wherein the second ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

29. (Amended) A semiconductor chip comprising:

a package having a plurality of pins; and

an electrostatic discharge (ESD) protection device connected to at least one of the pins,

the protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

33. (New) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region.

34. (New) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate; and

an implant within the substrate, the implant including two implant regions spaced apart by only the substrate region, wherein the substrate comprises a first conductivity type and the two implant regions comprise a second conductivity type, wherein conductivity between the two implant regions is not controlled by voltage potential of a gate above the two implant regions.

35. (New) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region such that an amount current flowing between the first and second doped regions is not controlled by a voltage potential of a gate above the first and second doped regions.